

Applic. No.: 10/062,049

Amdt. Dated January 31, 2005

Reply to Office action of November 5, 2004

Amendment to the drawings:

The attached sheets of drawings include changes to Figs. 1-3. These sheets replace the original sheets. In Figs. 1 and 2, previously omitted reference sign 20 has been added. In Fig. 3, a legend --Prior Art-- has been added.

Attachment: Replacement Sheets

Annotated Sheets Showing Changes

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REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-2, 4-5, 7-10, and 12 remain in the application.

Claims 1-2, 4-5, 7-10, and 12 have been amended. Claims 3, 6, and 11 have been cancelled.

In deference to the Examiner's requirement in item 1 on page 2 of the Office action, a legend --Prior Art-- has been added to Fig. 3.

In item 2 on page 2 of the above-identified Office action, the drawings have been objected to under 37 CFR 1.84(p)(5) as not showing the reference sign 20 mentioned in the specification.

The reference sign 20 has been added to Figs. 1 and 2.

In item 4 on page 3 of the above-mentioned Office action, claims 1, 3-6, 8, and 11 have been rejected as being anticipated by Fujimaki (JP 2-284452) under 35 U.S.C. § 102(b).

In item 6 on pages 3-4 of the above-mentioned Office action, claims 2, 7, and 9-10 have been rejected as being unpatentable

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over Fujimaki in view of Tanimura et al. (US Pat. No.
6,441,312 B1) under 35 U.S.C. § 103(a).

The rejections have been noted and claims 1 and 4 have been amended in an effort to even more clearly define the invention of the instant application. More specifically, the feature of claim 3 has been added to claim 1 and the features of claims 1 and 6 have been added to claim 4. Claims 3, 6, and 11 have been cancelled.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

a heat dissipation means arranged in a gap between said lower surface of said memory device and said upper surface of said board;

said heat dissipation means including an area of said board at which solder varnish covering said board is removed; and

said memory device bordering said board in said area.

Claim 4 calls for, inter alia:

a heat dissipation means arranged in a gap between said lower surface of said memory device and said upper surface of said board;

said heat dissipation means including a metal layer; and

said metal layer being connected to a conductive trace.

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Claim 1 of the instant application has been amended to incorporate the feature of claim 3 and to further define that the heat dissipation means is arranged in a gap between a lower surface of the memory device and an upper surface of the board, as can be derived from Figs. 1 and 2 and from the last paragraph on page 4 of the specification. Additionally, claim 3 also defines that the dissipation means includes an area on the upper surface of the board which does not have solder varnish thereon, and that the memory device borders the board in the area.

Additionally, claim 4 has been amended to incorporate the features of claims 1 and 6 and to further define that, again, the heat dissipation means is arranged in the gap between the memory device and the board and to additionally define that the metal layer is connected to a conductive trace.

With regard to amended claim 1, it is noted that none of the references discloses a heat dissipation means between the lower surface of the memory device and the upper surface of the board that is formed by an area in which the solder varnish of the board is removed. As is specified in the specification of the instant application, the problem with this kind of solder varnish is that it has a poor thermal conductivity (see the first paragraph, page 5), so that arranging the memory device

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directly on the board without the varnish provided thereon allows for a better heat dissipation from the memory device into the board. Fujimaki clearly does not disclose such a feature. In Fig. 2 of Fujimaki, it is clearly shown that the solder layer 6 is still provided between the respective device 2 and the board 1. Also Tanimura et al. do not disclose such a feature. It can be clearly seen from Fig. 2 and the other figures of Tanimura et al. that a solder layer 18 is arranged between the device 26 and the board.

Additionally, the remaining references cited but not applied by the Examiner also do not disclose the inventive feature as recited in amended claim 1 of the instant application, namely the direct attachment of the memory device on a surface portion of the board where the solder varnish usually provided there is removed.

With regard to amended claim 4, it is noted that none of the references discloses the feature of providing the heat dissipation means by a metal layer, which is connected to a conductive trace. This arrangement is clearly advantageous, as it provides not only for the heat dissipation means in the form of an isolated metal layer but also uses the thermal properties of conductive traces provided on the board for a carrying signal so that heat directed from the device to the metal layer

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is further spread via the conductive traces without the need for providing additional heat dissipation means. Thus, the heat dissipation area can be increased in a simplified manner.

Fujimaki provides heat radiating patterns 3. However, first of all, they are not provided in the gap between the memory device and the board and, further, they are not connected to any conductive traces, as is evident from the figures. The same is true for the disclosure of Tanimura et al. It can be clearly seen from the figures relating to the solder pattern between the board and the device (see Fig. 1 for example) that these patterns are not connected to any conductive traces.

The remaining references, cited but not relied upon by the Examiner, also do not disclose such a feature of amended claim 4. All references appear to disclose that in cases in which metal layers are used, they are "isolated" from any signal carrying traces or conductors.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 and 4. Claims 1 and 4 are, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claims 1 or 4, they are believed to be patentable as well.

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Applicants acknowledge the Examiner's statement in item 7 on page 4 of the above-mentioned Office action that claim 12 would be allowable if rewritten in dependent form including all of the limitations of the base claim and any intervening claims.

Claim 12 has been written in independent form including all of the limitations of the base claim and any intervening claims.

In view of the foregoing, reconsideration and allowance of claims 1-2, 4-5, 7-10, and 12 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to

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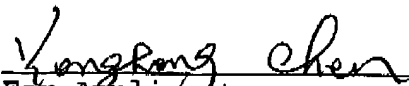
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the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

YC

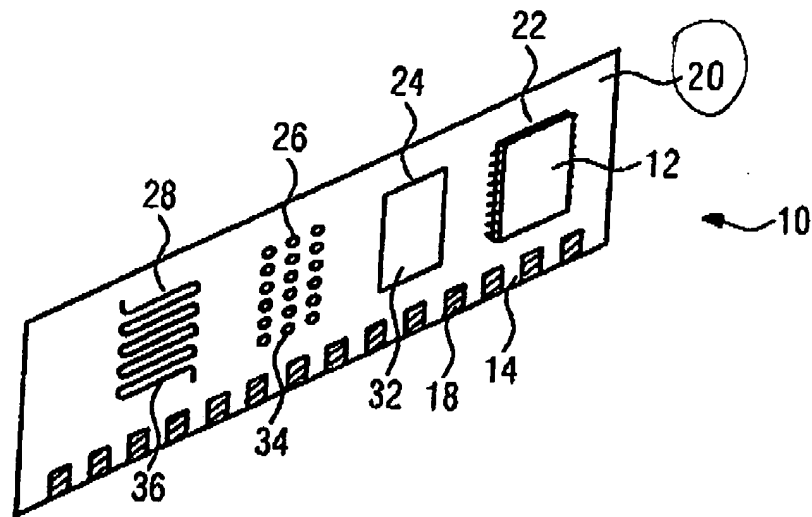
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Annotated Sheet Showing Changes

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FIG 1



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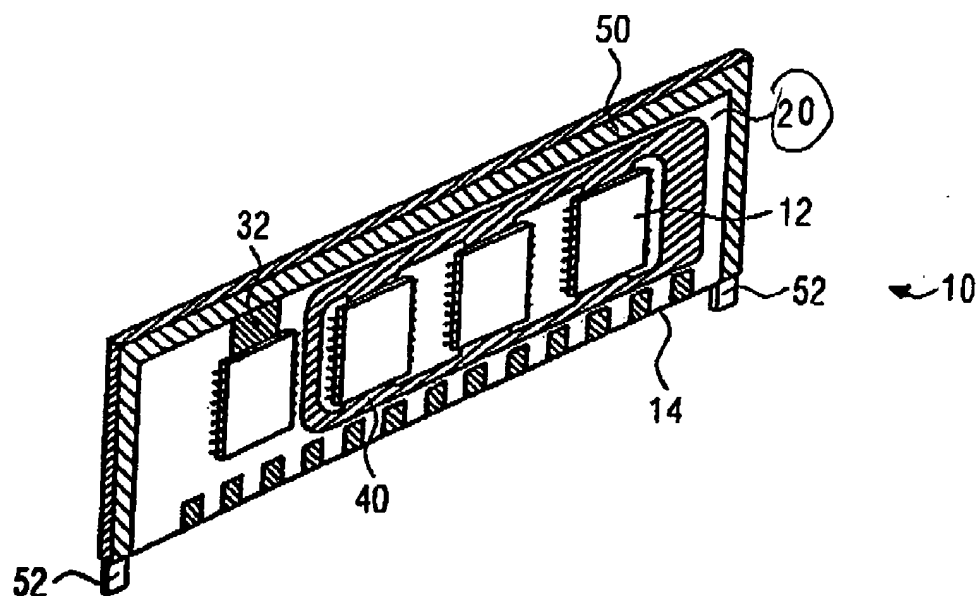
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FIG 2



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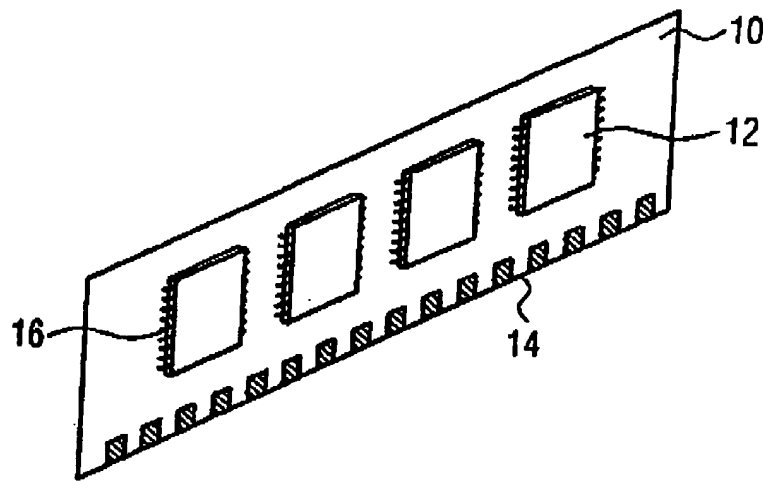
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FIG 3



PRIOR ART